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Technical Note TN-212 **Version 1.1**

Technical Product Information for the DAP 4200a ™

The DAP 4200a/526 model

- has an Intel i486 DX4 processor onboard
- provides 14-bit A/D converter resolution
- works with the 5V PCI bus for Pentium/Pentium II platforms
- comes with 16M of DRAM onboard memory
- transfers data to PC at high rates — up to 3.2M samples per second
- offers low latency—0.2 ms task time quantum—for fast response
- offers sampling period resolution to 100 ns
- samples or updates the digital section at up to 1.66 million values per second
- samples analog inputs at up to 769K samples per second at 12-bit accuracy
- updates analog outputs at up to 833K samples per second each
- provides onboard emulation of DSP routines
- provides the same input and output voltage ranges as the DAP 3200a
- allows fast real-time processing
- is compatible with other a-Series boards
- has expandable analog and digital inputs/outputs
- complies with the European EMC Directive and is CE marked.

There is only one DAP 4200a model: the DAP 4200a/526. This technical note describes features and architecture of the DAP 4200a.

The DAP 4200a provides 14-bit A/D resolution for its 16 onboard analog inputs, and 12-bit D/A resolution for its 2 onboard analog outputs. The onboard analog input channels sample at an overall 769k samples per second at 12-bit accuracy, and sample at 588k samples per second at 14-bit accuracy. The 16 onboard digital input channels sample at an overall rate of 1.66M words per second.

The DAP 4200a has a PCI host interface, and is capable of high speed data transfers to the host PC. The DAP 4200a requires a 5V 32-bit PCI slot. Using bus mastering DMA transfers, the DAP 4200a can transfer data to the host PC at 3.2M samples per second. This transfer rate is more than three times faster than that of the DAP 3200a.

The onboard multitasking operating system, DAPL™, runs on the DAP 4200a, and ensures that hardware-level differences are transparent. DAPL 2000 is a complete software environment for real-time data acquisition. Tasks that perform averaging, triggering, PID control, fast Fourier transforms, filtering, arithmetic operations and many other functions are pre-coded in DAPL. These tasks are chained together to form a complete data acquisition application. To aid application development, DAPL has many system diagnostics in addition to automatic memory and system checks that are done at initialization.

Much of the DAP 4200a design is similar to that of the DAP 3200a/415. The DAP 4200a uses the same type of analog and digital connectors as the DAP 3200a, so the DAP 4200a is compatible with all the same cabling and external boards for termination and expansion. Accessories used with any a-Series Data Acquisition Processor™ can be used with the DAP 4200a.

The DAP 4200a provides the same level of processing performance as the DAP 3200a/415, but offers more memory. The DAP 4200a has an onboard Intel 486 DX4 processor running at 96MHz, and has 16Mbyte of memory. The PCI bus allows the DAP 4200a to transfer data to the PC at high rates – up to 3.2M samples per second.

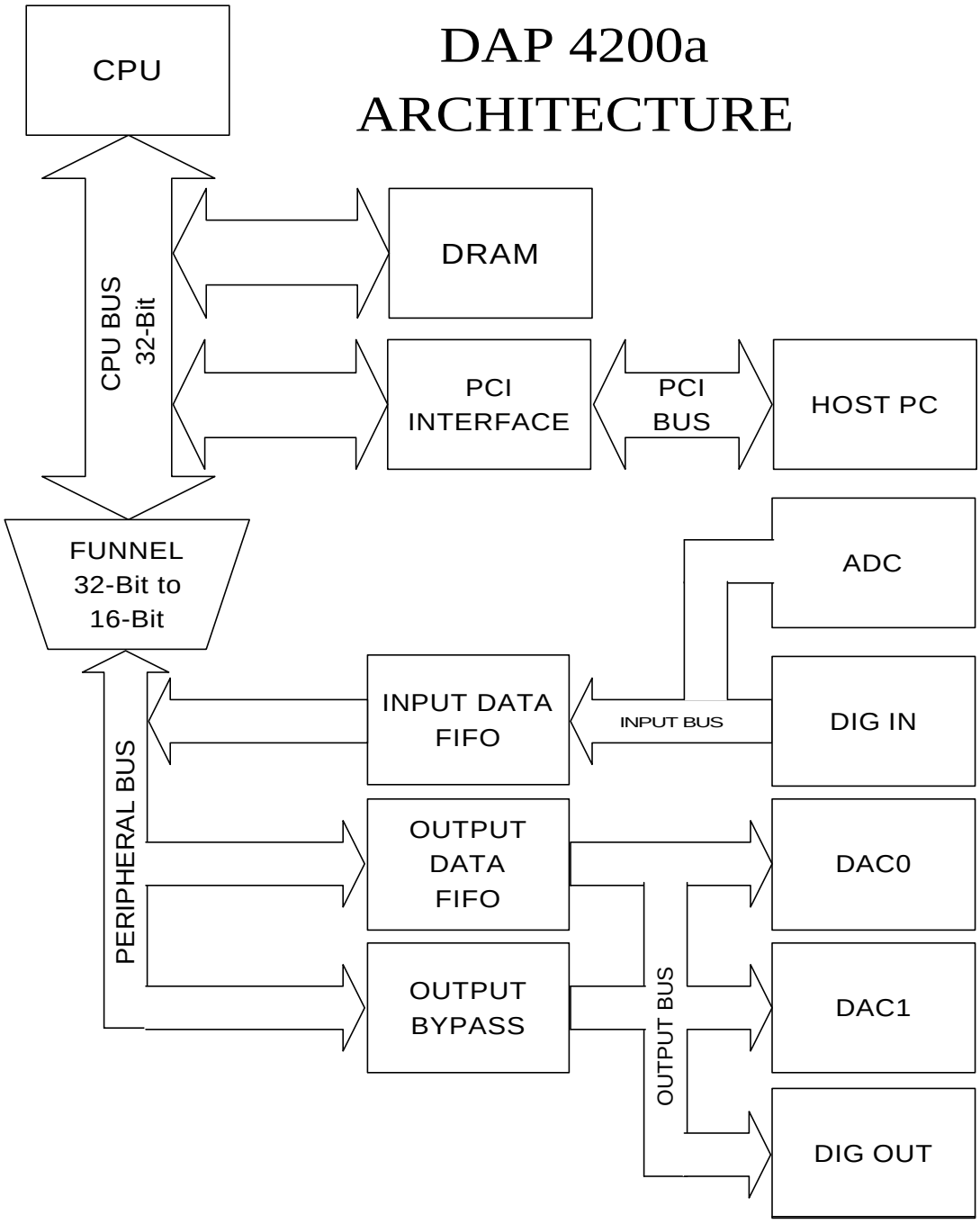

Figure 1: DAP 4200a Data Acquisition Hardware

Figure 1 displays the hardware architecture of the DAP 4200a. The figure shows that the PCI host interface is connected directly to the processor bus. This intimate connection allows fast and efficient data transfers

to the host PC. The figure also shows the two FIFOs on the DAP 4200 that handle data acquisition. The data FIFOs are unidirectional, buffering data for input and output.

Data are acquired or updated via dedicated hardware clocking circuitry at a rate of up to 1.66 million samples per second. Acquisition is clocked at a sampling rate or output rate controlled in software, and the rate is accurately maintained by onboard crystal-controlled timers. The sample period is specified with a resolution of 100 nanoseconds and the sample rate is accurate to 50 parts per million.

In addition to onboard timing, the DAP 4200 also has provisions for external triggering and clocking for the input and output sections. The DAP 4200a has an improved input sampling pipeline. Data are sampled and read by the processor in the same input clock cycle.

The 16-bit digital input port and the analog-to-digital converter are attached to the Input Data FIFO, one of the unidirectional data FIFOs. The maximum aggregate sample rate is 1.66M samples per second. Digital input alone can run at up to 1.66M samples per second. The maximum analog input sample rate is 769K samples per second.

The digital output port and the two analog outputs are attached to the Output Data FIFO. The maximum aggregate update rate is 1.66M updates per second. Digital output alone, like digital input, can run at up to 1.66M updates per second. Each of the analog outputs can be updated at 833K updates per second.

The Bypass section shown in Figure 1 allows the processor to asynchronously update either the digital or analog outputs. This means that periodic timing is not guaranteed, rather the processor will attempt to update the outputs whenever a time slice for this task becomes available. This is useful in control application where a digital output, for example, needs to open or close a valve at irregular intervals.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 4200a are provided in Table 1 below.

Table 1: DAP 4200a Typical Hardware Specifications
Preliminary

Specification	**DAP 4200a/526**
Dimensions	12.28” x 4.2”
Weight	11.5 oz
CPU type	Intel 80486DX4
CPU clock speed	96 MHz
CPU DRAM	16 Mbytes
Bus support	PCI
PC interface hardware	PCI interface
PC transfer mode	Bus Mastering
Maximum transfer rate	3.2 M samples/sec
Power requirements	+5V, 3.0 Amps
Operating temperature	0-50° C
Accuracy of crystal clocks	50 parts per million
Type of A⇒D converter	Successive Approximation
Model of A⇒D converter	Linear Tech LTC1419
Max. analog sampling rate[1] Gain = 1 Gain = 10 Gain = 100 Gain = 500	 769 K samples/sec 125 K samples/sec 25 K samples/sec 2 K samples/sec
Number of analog channels	16
Expandable to	512
Input voltage ranges	0 to 5 V; -2.5 to 2.5 V; -5 to 5 V; -10 to 10 V
Resolution -5 to 5 V range	14 bits 0.61 mV
Accuracy -5 to 5 V range	±1 LSB ±0.61 mV
Non-linearity	0.012%
Input bias current	12 nA
Analog input impedance	>> 10 MΩ
Common mode rejection	90 dB
Type of D⇒A converter	Voltage Output
Model of D⇒A converter	Analog Devices AD767
Maximum analog update rate[2]	833K updates/sec
Max. input voltage (fault-protected multiplexers)	±25V

Table 1: DAP 4200a Typical Hardware Specifications, continued

[1] The sampling rates are for 12-bit accuracy. The gain 1 sampling rate for 14-bit accuracy is 588k samples/sec.

[2] The DAP 4200a can update each of its two standard analog outputs independently at 833K updates per second. When analog output expansion is used, the update rate for expanded channels is determined by the maximum update rate of the digital port.

Expanded Analog Output Rate = 1.6M / (4 * Number of Channels)

Number of output channels	2
Expandable to	66
Output ranges	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V
Resolution -5 to 5 V range	12 bits 2.4 mV
Accuracy -5 to 5 V range	±1 LSB, ±2.4 mV
Analog output signal to noise ratio	0.0002% of full scale
Output impedance	0.05 Ω
Current source maximum	±1 mA
Digital output logic	FCT TTL
Digital input logic	FCT TTL
Maximum digital update rate[3]	2M words/sec
Number of input bits Number of output bits	16 16
Expandable to	128 input bits and 1024 output bits
Digital input Min. logical high Max. logical low Max. current sink Max. current source	 2 V 0.8 V 5 µA 5 µA
Digital output Min. logical high Max. logical low Max. current sink Max. current source	 2.6 V 0.5 V 12 mA 15 mA
External clock input min. pulse width	25 ns
External trig. input min. pulse width	60 ns
Trigger modes	GATED ONE-SHOT

[3] This figure is the maximum throughput of simultaneous digital input and output. Either digital input or digital output operating alone can maintain a throughput of 1.6 M words/sec.