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Technical Note TN-105 **Version 1.0**

Technical Product Information for the DAP 3000a™

The DAP 3000a models

- have a Texas Instruments 486 processor onboard.
- come with 512K or 2M of DRAM onboard memory.
- are compatible with other a-Series boards.
- work with the PC/AT ISA bus for 286/386/486/Pentium PC platforms.
- transfer data to the PC at high rates — up to 833K samples per second.
- allow fast real-time processing.
- offer low latency — 0.2 ms task time quantum — for fast response.
- have a sampling period resolution of 100 ns.
- provide onboard DSP routines.
- sample or update digital I/O at up to 1.66 million values per second.
- sample analog inputs at up to 769K samples per second.
- update analog outputs at up to 833K samples per second.
- have expandable analog and digital inputs/outputs.

There are two DAP 3000a models: the DAP 3000a/111 and the DAP 3000a/212. They vary in memory size and CPU type and speed. This technical note describes the DAP 3000a in terms of its similarities with other Data Acquisition Processor™ boards, software speed and functionality, and hardware characteristics.

The DAP 3000a is among the higher performance Data Aquisition Processors produced by Microstar Laboratories. The DAP 3000a is compatible with the DAP 3200e™ boards, with the exception of the analog I/O connector. The DAP 3000a uses a 68-pin analog connector, which is compatible with the DAP 1216e™ and DAP 2416e™. All configurations use the same termination and expansion boards whether the Data Acquisition Processor is a DAP 1216e, DAP 2416e, or DAP 3000a.

The DAP 3000a uses DAPL 2000™, a 32-bit version of DAPL™, the onboard multitasking operating system. DAPL is a complete software environment for real-time data acquisition. To aid application development, DAPL comes complete with many system diagnostics in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, PID control, fast Fourier transforms, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data aquisition application. Custom commands can also be written with the Developer's Toolkit for DAPL™ if multiple commands need to be combined, or if a specific application cannot be implemented with standard DAPL commands. On the next page, some standard DAPL commands are tabulated with a comparision of their speed of execution on the DAP 3000a/212 and DAP 2400e™/6.

Another common element among the a-Series and e-Series boards is the bus interface. Like every e-Series Data Acquisition Processor, the DAP 3000a is compatible with the PC/AT ISA bus for

286/386/486/Pentium industry standard platforms. Dual 1K word BiFIFO buffers allow fast data transfer to and from the host PC.

The main difference between the DAP 3000a and DAP 3200e series boards is that the DAP 3000a has an onboard Texas Instruments 486 processor while the DAP 3200e has an Intel 486 processor. The Intel processors have a 32-bit internal and external bus, while the Texas Instruments processor has a 32-bit internal bus and a 16-bit external bus.

The DAP 3000a is an excellent choice for applications where there is a need for a moderate amount of real-time processing of data in the time interval between samples, and for applications requiring fast sample rates. The DAP 3000a/212 features a clock-doubled processor that executes two internal clock cycles for each external clock cycle. The Texas Instruments 486 processor also features a hardware multiplier, making it well suited for DSP operations. The processor used on the DAP 3000a/212 has a larger cache than that used on the DAP 3000a/111 which further improves the performance of the DAP 3000a/212.

The TI 486 processor gives the DAP 3000a low latency—down to a 0.2 ms task time quantum. This means that when low latency mode is enabled, a single task will run for no more than 0.2 ms before DAPL switches to another task. This is crucial for process control applications where data must be responded to as quickly as possible.

Table 1: Comparison of DAPL command speeds — DAP 2400e/6 and DAP 3000a/212

DAPL Command	Description	Time of Execution[1] on 2400e/6	Time of Execution[i] on 3000a/212
`AVERAGE`	Averages groups of 120 data points	3.4 µs	0.8 µs
`FFT`	FFT of blocksize of 1024 points, amplitude spectrum	12.4 ms	6.8 ms
DAPL Expression: `P3 = P1 * P2`	Arithmetic operation, scales input magnitude	54 µs	5.2 µs
`LIMIT/WAIT`	Generates/processes level-based triggers	3.8µs	1.0 µs
`INTERP`	Interpolates 2 vectors	55.9 µs	4.4 µs

[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation. Kernel speeds for the task are smaller.

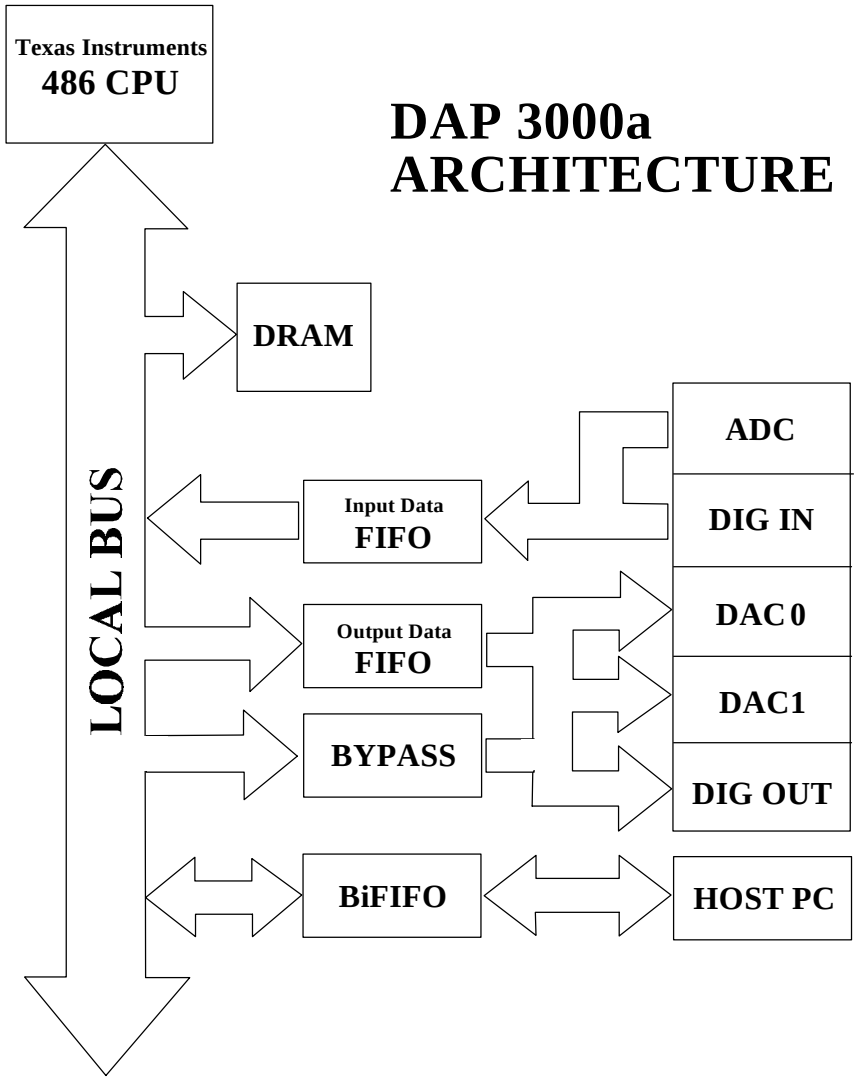

Figure 1: DAP 3000a Data Acquisition Hardware

From the point of view of DSP-intensive applications, the main difference between the DAP 3000a and the DAP 2400e is that, while the DAP 3000a has a 486 processor, the DAP 2400e has a 80C186 processor and a DSP coprocessor. The DAP 3000a handles DSP routines in the 486 processor. While it may seem that a dedicated DSP coprocessor would process DSP routines faster than a 486, the DAP 3000a/212 is as fast or faster than the DSP coprocessor in almost all cases. For non-DSP commands, the DAP 3000a is about four to sixteen times faster than the DAP 2400e. In general, the DAP 3000a/212 provides higher performance and is better suited to an application than a DAP 2400e.

In addition to high performance processing, the DAP 3000a provides the standard arrangement of complete analog and digital input and output sections. These analog and digital sections are completely expandable —see Table 2 for complete specifications.

Figure 1 displays the architecture of the internal processing hardware of the DAP 3000a. The figure shows the three FIFOs on the DAP 3000a that handle data acquisition and communications. The BiFIFO on the DAP 3000a handles communications between the Data Acquisition Processor and the PC. Information can be sent in both directions simultaneously, and can be either DAPL files, binary or text data, error messages, or DAPL system commands. In addition to the BiFIFO for communications, there is an output data FIFO and an input data FIFO. The data FIFOs are unidirectional, buffering data for either input or output.

Data are acquired or updated via dedicated hardware clocking circuitry at a rate of up to 1.66 million samples per second. Acquisition is clocked at a sampling rate or output rate controlled in software, and the rate is accurately maintained by onboard crystal-controlled timers. The sample period is specified with a resolution of 100 nanoseconds. The sample rate is accurate to 50 parts per million.

In addition to onboard timing, the DAP 3000a also has provisions for external triggering and clocking for the input and output sections. Software triggering is provided in DAPL, providing pre-trigger as well as post-trigger data and allowing complex trigger events.

The 16-bit digital input port and the analog-to-digital converter are attached to the input data FIFO, one of the unidirectional data FIFOs. The maximum aggregate sample rate is 1.66M samples per second for the DAP 3000a/212 and 333K samples per second for the DAP 3000a/111. Digital input alone can run at up to the maximum aggregate sample rate. The maximum analog input sample rate for the DAP 3000a/212 is 769K samples per second and for the DAP 3000a/111 is 333K samples per second.

The digital output port and the two analog outputs are attached to the output data FIFO. The maximum aggregate update rate is 1.66M updates per second for the DAP 3000a/212 and 333K update per second for the DAP 3000a/111. Digital output alone, like digital input, can run at up to the maximum aggregate sample rate. Each of the analog outputs can be updated at 833K updates per second on the DAP 3000a/212 and at 333K samples per second on the DAP 3000a/111.

The 486 processor bus on the DAP 3000a gives a maximum bandwidth of 2M words—or samples—per second of input/output for data. An example of using this maximum bandwidth is a situation where both input sampling and output updating occur. In this example, two channels of digital data and one channel of analog data could be acquired at 330K samples per second, the digital port could be updated at a rate of 330K updates per second, and two analog outputs could each be updated at a rate of 330K updates per second. Other mixes of sampling and update rates may be used, as long as the total throughput for input or output does not exceed 2M words per second.

The Bypass section shown in Figure 1 allows the 486 processor to asynchronously update either the digital or analog outputs. This means that periodic timing is not guaranteed, rather the 486 processor will attempt to update the outputs whenever a time slice for this task becomes available. This is useful in control application where a digital output, for example, needs to open or close a valve at irregular intervals.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 3000a are given below in Table 2.

Table 2: DAP 3000a Typical Hardware Specifications

Specification	DAP 3000a/111	DAP 3000a/212
Dimensions	13.33" x 4.8"	13.33" x 4.8"
Weight	10.2 oz	10.2 oz
CPU type	TI 486SLC/E	TI 486SXLC2
CPU clock speed	24 MHz	48 MHz
CPU DRAM	512 Kbytes	2 Mbytes
Cache size	1 Kbyte	8 Kbytes
Bus support	ISA AT	ISA AT
PC interface hardware	dual 1 KWord biFIFO buffers	dual 1 KWord biFIFO buffers
PC transfer mode	I/O Interrupt	I/O Interrupt
Maximum transfer rate	333K samples/sec	833K samples/sec
Power requirements	+5V, 2.0 Amps	+5V, 2.0 Amps
Operating temperature	0-50 °C	0-50 °C
Accuracy of crystal clocks	50 parts per million	50 parts per million
Type of A⇒D converter	Successive Approximation	Successive Approximation
Max. analog sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 333 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s	 769 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s
Number of analog input channels	16	16
Expandable To	512	512
Input voltage ranges	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V[2]	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V[2]
Resolution -5 to 5 V range	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy -5 to 5 range	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV
Non-linearity	0.05%	0.05%
Input bias current	12 nA	12 nA
Analog input impedance	>> 10 MΩ	>> 10 MΩ
Common mode rejection	90 dB	90 dB
Max. analog input voltage	±25 V	±25 V
Type of D⇒A converter	Voltage Output	Voltage Output
Model of D⇒A converter	Analog Devices AD767	Analog Devices AD767

[2] There is a maximum speed reduction for the ±10 volt input range on the DAP 3000a™/212; using the input voltage range of ±10 at Gain = 1, the maximum sampling speed is approximately 417K samples per second. The DAP 3000a™ /111 sampling speed is not affected by the voltage range.

Specification	DAP 3000a/111	DAP 3000a/212
Maximum analog output update rate[3]	333K updates/sec	833K updates/sec
Number of channels	2	2
Expandable to	66	66
Output ranges	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V[3]
Resolution -5 to 5 V range	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy -5 to 5 V range	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV
Analog output signal to noise ratio	0.0002% of full scale	0.0002% of full scale
Output impedance	0.05 Ω	0.05 Ω
Current source maximum	±1 mA	±1 mA
Digital output logic	FCT TTL	FCT TTL
Digital input logic	FCT TTL	FCT TTL
Maximum digital update rate[4]	333K words/sec	1.6M words/sec
Number of input bits Number of output bits	16 16	16 16
Expandable to	128 input bits and 1024 output bits	128 input bits and 1024 output bits
Digital input Min. logical high Max. logical low Max. current sink Max. current source	 2 V 0.8 V 5 µA 5 µA	 2 V 0.8 V 5 µA 5 µA
Digital output Min. logical high Max. logical low Max. current sink Max. current source	 2.4 V 0.5 V 12 mA 15 mA	 2.4 V 0.5 V 12 mA 15 mA
External clock input min. pulse width	25 ns	25 ns
External trig. input min. pulse width	60 ns	60 ns
Trigger modes	GATED ONE-SHOT	GATED ONE-SHOT

[3] The DAP 3000a/212 can update each of its two standard analog outputs independently at 833K updates per second. When analog output expansion is used, the update rate for expanded channels is determined by the maximum update rate of the digital port.

Expanded Analog Output Rate = 1.6M / (4 * Number of Channels)

[4] This figure is the maximum throughput of simultaneous digital input and output. Either digital input or digital output operating alone can maintain a throughput of 1.6 M words/sec for the DAP3000a/212.