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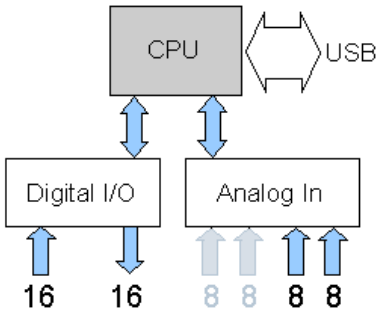
xDAP 7420

Features

- Self-contained, with USB connectivity to host
- 8 analog-to-digital converter devices clocked simultaneously
- 1 million samples per second capture on each converter
- 8 million samples per second sustainable aggregate capture
- 8 million samples per second sustainable USB transfer rate
- 16 multiplexed analog differential input channels
- Optional expansion panels for BNC input connectors
- 16-bit resolution on each channel, no missing codes
- Input voltages ranges from ± 0.1 to ± 10.0 volts
- Superior measurement repeatability > *14 ENOB*
- CE and 50Hz compliant for European applications
- Programmable sampling interval at resolution 0.02 microseconds
- Autonomous sampling controlled by 2 GHz Intel® processor
- Onboard storage for a minute of buffered data at *maximum rates*
- Script-configurable through onboard DAPL 3000 operating system

(1) *Intel* is a trademark of the *Intel Corporation*.

Block Diagram



xDAP 7420 Specifications

Physical Characteristics

Parameter	Sym	Min	Typ	Max	Units
Enclosure					
Length, body			12.43 (31.6)		in (cm)
Length, body plus handles			14.25 (36.2)		in (cm)
Width			9.25 (23.5)		in (cm)
Height, body			5.25 (13.3)		in (cm)
Height, body plus feet			5.56 (14.1)		in (cm)
Weight			11.75 (5.3)		lb (kg)
Operating temperature (1)	T_a	0	—	50	°C
External AC Power Requirements					
Supply input voltage (2)	V_{ps}	100 —	115 230	— 240	V RMS V RMS
Supply input current	I_{ps}		— —	6 3	A RMS (115V) A RMS (230V)
Supply input power (3)	P_{ps}	10	50	100	W
Supply input frequency (4)	f_{ps}	47 57	50 60	53 63	Hz
Internal DC power capacity					
Continuous ground current load capacity				100	mA
Fuse rating, +5V supply Fuse rating, digital gnd Fuse rating, digital+5V			2 2 2		A

(1) Presumes adequate ventilation.
(2) The full range from 100 to 240 volts is tested.
(3) Does not include loading from added termination networks or customizations.
(4) Min and max frequency limits are the tested range, nominal value ± 6% tolerance

Processor Module

Feature	Property
Processor type	Intel® Celeron 575
Processor clock speed	2.0 GHz
Processor main memory	1.0 GB
Embedded operating system	DAPL 3000

Timing Characteristics

Parameter	Sym	Min	Typ	Max	Units
Sampling interval resolution	Δt_S		20		ns
Sampling interval range	t_S	0.5		10000.0	µs
Timing absolute accuracy (1)		50	—	50	PPM
Sampling interval jitter		—	100	—	ps
Acquisition latency (2)		—	—	900	ns

(1) Oscillator is affected by temperature, supply, and long-term drift variations.
(2) Describes hardware performance only. Buffering, processing, and data transport contribute much larger latencies.

Input Characteristics

Feature	Property
Analog input channel type	Differential
Number of analog-to-digital converters (1)	8 (simultaneous)
Maximum multiplexed analog input signals	32
Primary HD connector	16 channels
Optional BNC input panels	8 or 16 channels
Analog-to-digital converter codes	65536 (16 bits)
Skipped or missing codes	none
Skipped or missing samples	none
Configurable input ranges	7

-10 V to +10 V	gain 1
-5 V to +5 V	gain 2
-2 V to +2 V	gain 5
-1 V to +1 V	gain 10
-0.5 V to +0.5 V	gain 20
-0.2 V to +0.2 V	gain 50
-0.1 V to +0.1 V	gain 100

(1) Conversion operations on all converters are clocked simultaneously.

Digital I/O Characteristics

Parameter	Sym	Min	Typ	Max	Units
Inputs					
Digital Input Ports: 1 (Asynchronous, 16 Input lines each)					
Absolute input range limits		-0.5		5.5	V
Operating range	V_i	0.0		5.0	V
Input for level-low	V_{iL}			0.8	V
Input for level-high	V_{iH}	2.0			V
Input current [1]	I_I	-12	—	12	µA
Input load [1]	R_i C_i	— —	10 120	— —	kΩ pF
Input transition time [2]	T_t			60	ns
Outputs					
Digital Output Ports: 1 (Asynchronous, 16 output lines each)					
Output voltage range	V_o	0		3.3	V
Continuous output current	I_o	-5		5	mA
Output voltage at -5 mA load	V_{oH}	2.4			V
Output voltage at 5 mA load	V_{oL}			0.4	V
Output termination [1]	R_T	—	10	—	kΩ
Output capacitive load [3]	C_L			200	pF
Unloaded switching transition time	t_{pd}		12	—	ns
Loaded switching transition time [4]	t_{pdL}		30	—	ns
Output voltage source					
Output supply voltage	V_{ss}	—	5.0	—	V

Regulation under full load	ΔV_{ss}	-5		+5	%
Supply current	I_{ss}			0.5	A
Ground sink current	I_G			-0.5	A

(1) The termination resistance is present at all times, and will pull voltages to ground under unpowered conditions.
(2) Signal transitions between V_{iL} and V_{iH} levels can go more slowly, but slower transitions could lead to uncertainty in captured value.
(3) Excessive capacitive loading can degrade device stability.
(4) Includes C_L capacitive loading in addition to termination.

Input Electrical Characteristics

Parameter	Sym	Min	Typ	Max	Units
Input channels					
Absolute input range limits	V_{iMax}	-35		+35	V
Operating input range limits (1)	V_i	-13		+13	V
Input impedance	R_i C_i	—	20 50	—	MΩ pF
Input leakage current	I_L	—	5	46	nA
Charge injection (2)		—	0.4	—	pC
Offset error (3)		-2	—	2	counts
Offset thermal sensitivity		—	—	—	µV / °C
Long term offset drift		—	—	—	% / yr
Gain error (3)		—	—	0.05	%
Gain thermal sensitivity		—	—	—	% / °C
Long term gain drift		—	—	—	% / yr
Slewing rate limit (4)		—	20	—	V / µs

(1) For accurate measurements through the full differential measurement range, the common mode must be restricted to the *Common Mode Voltage Range* (CMVR), a subset of the maximum operating range. The CMVR equals the maximum operating range minus the configured differential range; in effect, this reserves half of the differential input range near each operating range limit.
(2) This injection occurs each time a multiplexer device captures a new sample.
Assumes a conventional input signal 0 V at 0 Ω.
(3) Assumes proper calibration and environment temperature regulated to 25 °C
(4) Does not cover the settling time that follows a slewing transient.

Dynamic Response Characteristics

Parameter	Sym	Min	Typ	Max	Units
Range -10V to +10V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	0.58	—	count
Signal to Noise Ratio [3]	SNR	—	90	—	dB
Total Harmonic Distortion [3]	THD	—	-90	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	87	—	dB
Effective Number of Bits [3]	ENOB	—	14.1	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	92	—	dB
Nonlinearity Error (Integral Noninearity)	INL			1.2	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-98	—	dB
Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-92	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-88	—	dB
Range -5V to +5V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	0.60	—	count
Signal to Noise Ratio [3]	SNR	—	89	—	dB
Total Harmonic Distortion [3]	THD	—	-94	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	88	—	dB
Effective Number of Bits [3]	ENOB	—	14.3	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	98	—	dB
Nonlinearity Error (Integral Noninearity)	INL			1.3	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-103	—	dB

Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-92	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-92	—	dB
Range -2V to +2V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	0.70	—	count
Signal to Noise Ratio [3]	SNR	—	85	—	dB
Total Harmonic Distortion [3]	THD	—	-95	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	85	—	dB
Effective Number of Bits [3]	ENOB	—	13.8	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	98	—	dB
Nonlinearity Error (Integral Noninearity)	INL			1.4	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-110	—	dB
Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-92	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-92	—	dB
Range -1V to +1V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	0.91	—	count
Signal to Noise Ratio [3]	SNR	—	87	—	dB
Total Harmonic Distortion [3]	THD	—	-91	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	86	—	dB
Effective Number of Bits [3]	ENOB	—	12.8	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	97	—	dB
Nonlinearity Error (Integral Noninearity)	INL			1.5	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-110	—	dB

Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-92	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-92	—	dB
Range -0.5V to +0.5V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	2.6	—	count
Signal to Noise Ratio [3]	SNR	—	79	—	dB
Total Harmonic Distortion [3]	THD	—	-91	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	78	—	dB
Effective Number of Bits [3]	ENOB	—	12.8	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	93	—	dB
Nonlinearity Error (Integral Noninearity)	INL			1.6	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-110	—	dB
Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-85	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-85	—	dB
Range -0.2V to +0.2V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	4.5	—	count
Signal to Noise Ratio [3]	SNR	—	74	—	dB
Total Harmonic Distortion [3]	THD	—	-91	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	74	—	dB
Effective Number of Bits [3]	ENOB	—	12.1	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	86	—	dB
Nonlinearity Error (Integral Noninearity)	INL			2.2	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-110	—	dB

Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-80	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-80	—	dB
Range -0.1V to +0.1V					
Theoretical quantization noise [1]			0.57		count
Static ground noise [1] [2]		—	7.6	—	count
Signal to Noise Ratio [3]	SNR	—	70	—	dB
Total Harmonic Distortion [3]	THD	—	-91	—	dB
Signal to Noise-and-Distortion [3]	SINAD	—	70	—	dB
Effective Number of Bits [3]	ENOB	—	11.4	—	bits
Spurious-Free Dynamic Range [4]	SFDR	—	80	—	dB
Nonlinearity Error (Integral Noninearity)	INL			2.6	count
Common Mode Rejection Ratio at DC	$CMRR_0$	—	-110	—	dB
Common Mode Rejection Ratio at 60 Hz	$CMRR_{60}$	—	-76	—	dB
Common Mode Rejection Ratio at 10 kHz	$CMRR_{10k}$	—	-76	—	dB

(1) Noise levels are given as RMS (standard deviation), where one unit corresponds to one LSB count of the converter.
(2) Quiescent noise is measured with constant input level, nominally held at 0 V through 0 Ω resistance, ignoring offset.
(3) Repeatability tests use 10 kHz, sinusoidal excitation with amplitude > -0.5 dB relative to full converter range, and sampling rate is 2×10^5 samples per second.
(4) Same as repeatability tests but sampling at 1.0×10^6 samples per second.

Terminology

Decibel

A logarithmic representation for the ratio of signal power in two signals. For each incremental increase of 10 decibels, the ratio increases by a power of 10. For each incremental decrease of 10 decibels, the ratio decreases by a power of 10.

Differential

A measurement scheme using an input amplifier having two balanced inputs, a *plus input* and a *minus input.* The amplifier responds in proportion to the difference between the plus input and minus input signals.

Common Mode

Voltages presented to the inputs of a differential amplifier can be decomposed into two parts, a *common mode* component that is halfway between the two input voltages, and a balanced *differential mode* component that is added or subtracted from the *common mode* component. When both inputs of a differential amplifier are connected to the same voltage signal, the amplifier is said to be driven *in common mode*. The ideal response of a differential amplifier to the common mode input component is zero.

Common Mode Rejection (Common Mode Rejection Ratio, CMRR)

The ratio of the signal power in the response of a differential amplifier driven in *common mode* to the signal power that would be observed when measuring the signal in a normal differential configuration.

Multiplexed Sampling

Analog to digital converters operate in a *multiplexed configuration* when multiple input signals are selected in succession by a digitally-controlled analog switch, and routed to an analog-to-digital converter. This strategy allows hardware devices to process more signal channels, but with the disadvantage that a longer sampling time interval is typically necessary to allow settling time after each switching transient.

Expansion

A strategy employed by Microstar Laboratories to increase the number of signal channels available with multiplexed sampling.

Resolution (Quantization)

The number of bits available to represent a digitally captured analog signal. The first bit is able to resolve the range into two parts: the positive half and the negative half. The next bit can resolve each of these halves into two parts, an upper and lower part. Continuing this process, N bits resolve the input range into 2^N distinct and equally-spaced sub-ranges.

Full Range

For a converter that can produce N distinct output codes, *full range* is used somewhat interchangeably to mean the full set of possible output codes, or the corresponding differential input voltage swing required to cover all of these output codes.

Dynamic Range

The range of signal levels that can be distinguished from the low-level noise floor. (See *Signal to Noise Ratio.*)

Conversion ratio

The ratio of the number of converter output codes to the input voltage range required to produce them. The *ideal* conversion ratio is the ratio of the number of converter output codes to the nominal input voltage range. The *actual* conversion ratio is the observed number of output codes divided by the voltage range that produces them. For a perfect conversion, the converter output values will exactly equal the input differential voltage times the ideal conversion ratio.

Offset Error (bias)

With a differential amplifier input driven in common mode, a consistent nonzero measurement is an *offset error.* Calibration is effective for nulling offset errors.

Gain Error

After correcting for offsets, the *gain error* is the difference between an observed conversion ratio and the ideal conversion ratio, normalized by the ideal conversion ratio. Calibration is effective for correcting gain errors.

Nonlinearity Error (Integral Nonlinearity Error, INL)

Nonlinearity error can be considered the component of digitization error that does not arise from random effects. After making a best correction for gain and offset errors, any non-random differences between actual conversion results and the results predicted by the conversion ratio are *nonlinearity errors.* Because the converter must quantize the measurement according to the number of available bits of resolution, a nonlinearity error of at least 0.5 bits is unavoidable.

Ground Noise (Static Noise, Background Noise, Noise Floor)

Random effects in conversion results reflect the combined effects of quantum noise in devices, radio frequency interference, and so forth. Noise effects cause a significant portion of the errors observed in digitized measurements. *Static* or *quiescent* noise is observed by measuring a steady reference voltage during periods of relative inactivity. *Dynamic ground noise,* also called *background noise* or *noise floor,* is observed during periods of intensive sampling activity in the presence of changing high-level input signals.

Signal to Noise Ratio (SNR)

The ratio of the signal power in a full-range sinusoidal input signal to the total power in the dynamic background noise. This is a measure of how much random effects interfere with measurement accuracy in each sample. It is a best-case estimate; background noise effects tend to remain about the same level while the signal power drops significantly as the magnitude of the signal is reduced below full scale.

Harmonic Frequencies (Harmonic Distortion)

Applying a nonlinear function to a pure sinusoidal input signal results in a distorted signal having additional frequencies at twice the original signal frequency, three times the original signal frequency, and so forth. The introduced frequencies are called *harmonics.*

Total Harmonic Distortion (THD)

With an input converter driven by a full-range sinusoidal input signal, *total harmonic distortion* is the ratio of the signal power in the sinusoidal input signal to the total signal power in the harmonic frequencies resulting from nonlinearity.

Spurious-Free Dynamic Range (SFDR)

With an input converter driven by a full-range sinusoidal input signal, the *spurious-free dynamic range* is the ratio of the sinusoidal input signal power to the signal power at any other frequency having the next-highest signal power. Most often, the spurious frequency is one of the harmonic frequencies caused by nonlinearity. Since the THD measurement includes several harmonic frequencies, but SFDR only includes one, the SFDR figures tends to be slightly higher.

Signal to Noise+Distortion Ratio (SINAD)

SINAD is ratio of the signal power in a full-range sinusoidal input signal to the total power in all other frequencies resulting from the conversion process. This is similar to SNR, except that the signal power in the harmonics is included along with the background noise. SINAD provides an estimate of measurement errors to expect from consistent and random effects in combination.

Effective Number of Bits (ENOB)

ENOB is an equivalent way to present SINAD in terms of powers of 2 and "bits" rather than decibels. An ENOB of 14 bits for a 16 bit converter can be loosely interpreted as meaning that variations can be expected in the last 2 bits of each conversion due to nonlinearity and random effects. Accuracy can be extended beyond the levels suggested by ENOB, however, if measurements are repeatable and averaging can be applied to reduce the random effects.

Settling Time (Transient Response)

When using multiplexed inputs or dedicated inputs subjected to large step transients, the drive current and bandwidth limitations of amplifiers prevent tracking of instantaneous step edges. *Settling time* describes the length of sampling interval t_s that should be allowed to give the conversion circuits time to reach the correct values within acceptable accuracy.

Slewing (Rate Limiting)

A condition in which an input amplifier is subjected to a large input level change and uses all available current internally for driving its output stage. This results in a fast *linear ramp* output behavior, rather than tracking the input change accurately. Sinusoidal waveforms with sufficiently large magnitude and frequency will be distorted if the time derivative of the waveform exceeds the *slew rate limit*.

Jitter

Variability in the times at which discrete events takes place. Jitter causes uncertainty about which precise moments a signal sample is captured or a switching event is detected.

Hold Time

The amount of time that a signal must be held at a constant level to be sure that other circuits will respond reliably.

Setup Time

An amount of time that must be allowed after sending a signal for changes to take effect.

Latency

A delay in receiving the results of a conversion. For example, a sample might require 1 microsecond to be transported from the converter device, 2 milliseconds to be moved to buffer memory, and 25 milliseconds to be transferred to host memory. The delays for receiving the data typically do not matter unless it is important to respond very quickly.

Crosstalk

A side effect of stray coupling between signal lines, resulting in small measurement changes that increase apparent correlation between signals measured on the lines. Such effects are typically introduced by capacitive and inductive coupling between lines that are physically close in cabling and on circuit boards.

Charge injection

An amount of charge capacitively coupled into converter inputs each time a signal is captured. Though the effects of each charge injection are very small, when the device is clocked at a very high rate, the cumulative effects act like a current flow, interacting with the input circuit impedance and producing an observable shift in the measurements of input signals.

Charge cross-injection

A contributor to crosstalk resulting from multiplexer operation. When connected to one line, stray capacitances at the switching device charge up to balance with the line voltage. When switched to a new signal source, the voltage on this capacitance is temporarily out of balance with the new line, causing a very small but rapid surge in charge until voltages again equalize. With poorly conditioned input signals, the effects can be amplified by high impedances and stray dynamics. The effects are greatest when multiplexer switching occurs at a high rate.

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